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10/723,309	11/26/2003	Christian Pacha	V0195.0004	6833

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EXAMINER	
LAM, TUAN THIEU	

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2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,309	PACHA ET AL.	
	Examiner	Art Unit	
	Tuan Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *25-32,34-37 and 39-53* is/are pending in the application.

4a) Of the above claim(s) *26 and 51* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25,27-32,34-37,39-50,52 and 53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 12/22/2008. Claims 25, 27-32, 34-37, 39-50 and 52-53 are under examination. Claims 26 and 51 have been withdrawn from consideration.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 25, 27-29, 34-37 and 45-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Inukai et al. (Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakeage-Free Giga-Scale Integration).

Figure 9 of Inukai et al. shows a circuit arrangement comprising an edge triggered flip flop comprising a storage flip flop subcircuit (six thick gate transistor on the right hand side coupled to high Vdd and ground potential) having a plurality of storage transistors with a threshold voltage of a first value (high threshold), a first power switch transistor (transistor receiving Standby signal) having a second threshold voltage (high threshold), wherein an application of a predetermined electrical potential (Standby signal) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which when at least one supply voltage(VSS) is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharged from the circuit arrangement, and a plurality of switching transistors (transistors within the set reset crossed

coupled NAND gates), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling a flip flop input signal (inputs applied to the NAND gates) into the storage flip flop subcircuit, wherein the magnitude of the first and/or second value is greater that the magnitude of the third value (high threshold voltage is larger than the low threshold voltage), wherein each one of the terminals of the switching transistors has a defined electrical potential in the operating state (in the standby mode, the source, drain and gate terminals of the switching transistors have a defined electrical potential), a pulse generator circuit (the circuit to the left of the crossed coupled NAND gates) that generates the flip flop input signal from an input signal (D) and from a clock signal (CLK) and is coupled to the first power switch transistor and to the switching transistor, wherein the pulse generator circuit is configured such that the flip flop input signal is precharged to a first electrical potential during a precharging clock signal phase (when the CLK is at logic low, the flip flop input signal is precharged to low Vdd), that the flip flop input signal is brought to a second electrical potential by a rising clock edge following the precharging clock signal phase, and that the state of the flip input signal is fixed after the rising clock edge as called for in claim 29.

Regarding claim 25, the storage flip flop subcircuit has two crossed coupled inverters.

Regarding claim 27, since the storage and the first power switching transistors have a higher threshold voltage than the switching transistors, the thickness of the gate insulating layer of the storage transistors and the first power switch transistor is greater than the thickness of the gate insulating layer of the switching transistors.

Regarding claim 28, since the storage transistor and the first power switching transistor have a higher threshold voltage than the switching transistors, the channel width of the storage

transistors and the first power switch transistor is less than the thickness of the gate insulating layer of the switching transistors.

Regarding claims 34-37, figure 9 shows the pulse generator comprises inverters having transistors with low threshold voltage.

Regarding claims 45-50, figure 9 shows the protection transistors (transistors receiving WL signal) having high threshold voltage.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 30-32 and 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inukai et al. (Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakeage-Free Giga-Scale Integration) in view of Matsuzaki et al. (USP 6,500,715).

Inukai et al. reference discloses an circuit arrangement having all the aspects of the present invention as noted in claim 29 except for a second power switch transistor coupled to the switching transistor as called for in claims 30-32 and 52-53.

Matsuzaki et al. reference figure 5 shows a power switch transistor (MN1/MP1) connected between a logic circuit having a plurality of switching transistors (TP1, TN1) and power supply. Such an arrangement is used to eliminate leakage current thus reducing power consumption (column 16, lines 19-67; column 20, lines 1-30). Therefore,

it would have been obvious to person skilled in the art at the time the invention was made to include an additional power transistor between the GNDV of a crossed coupled NAND gate which having a plurality of transistors and the power supply (ground potential) for the purpose of reducing power consumption.

5. Claims 39-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inukai et al. (Boosted Gate MOS (BGMOS): Device/Circuit Cooperation Scheme to Achieve Leakeage-Free Giga-Scale Integration) in view of Sani et al. (USP 6,794,914).

Inukai et al. reference discloses an circuit arrangement comprising all the aspects of the present invention as noted in the above except for the test circuit coupled to the flip flop for testing the functionality of the flip flop as called for in claim 39.

Sani et al. shows a flip flop having a test circuit (310 of figure 3) to test and to enhance the reliability of the flip flop. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to include Sani et al.'s test circuit in the circuit arrangement of Inukai et al. for purpose of enhancing the reliability of the edge triggered flip flop.

Regarding claim 40, the combination of Inukai et al. and Sani et al. show the test circuit comprising a test input signal (Sin), output components (output of the flip flop) that reads a test output signal of the flip flop.

Regarding claim 41, the combination of Inukai et al. and Sani et al. show the test circuit comprising a plurality of transistors (322, 324) having a high threshold voltage.

Regarding claim 42, since test transistors have a higher threshold voltage than the threshold voltage of the switching transistors, the thickness of the gate insulating layer of the test transistors are greater than the thickness of the gate insulating layer of the switching transistors.

Regarding claims 43-44, since test transistors have a higher threshold voltage than the threshold voltage of the pulse generator's transistors, the thickness of the gate insulating layer of the test transistors are greater than the thickness of the gate insulating layer of the pulse generator's transistors.

6. Claims 25, 27-32, 34-37 and 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oklobdzija et al. (USP 6,232,810) in view of Matsuzaki et al. (USP 6,500,715).

Figure 6 of Oklobdzija et al. shows a circuit arrangement comprising an edge triggered flip flop comprising a storage flip flop subcircuit (32) having a plurality of storage transistors with a threshold voltage of a first value (3.2 micron, high threshold), and a plurality of switching transistors (34, 36) having a threshold voltage of a third value (16micron), wherein each one of the terminals of the switching transistors has a defined electrical potential in the operating state, a pulse generator circuit (101) that generates a flip flop input signal from an input signal (D) and from a clock signal (CLK) and is coupled to the switching transistor, wherein the pulse generator circuit is configured such that the flip flop input signal is precharged to a first electrical potential during a precharging clock signal phase, that the flip flop input signal is brought to a second electrical potential by a rising clock edge following the precharging clock signal phase, and that the state of the flip input signal is fixed after the rising clock edge.

What not shown in Oklobdzija et al.'s figure 6A is the high threshold voltage power switch couple/decouple the pulse generator to/from the ground potential in response to a standby signal as called for in claim 29.

Matsuzaki et al. reference figure 4 shows a high threshold voltage power switch transistor (MN1/MP1) couple/decouple a logic circuit having a plurality of switching transistors (TP1, TN1) to/from a power supply/ground potential. Such an arrangement is used to eliminate leakage current thus reducing power consumption (column 16, lines 19-67; column 20, lines 1-30). Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include a high threshold power transistor for coupling/decoupling the pulse generator of Oklobdzija et al. to/from the power supply/ground responsive to a standby signal for the purpose of reducing power consumption.

Regarding claim 25, the storage flip flop subcircuit 32 of Oklobdzija et al. reference has two crossed coupled inverters.

Regarding claim 27, since the storage and the first power switching transistors have a higher threshold voltage than the switching transistors, the thickness of the gate insulating layer of the storage transistors and the first power switch transistor is greater than the thickness of the gate insulating layer of the switching transistors.

Regarding claim 28, since the storage transistor and the first power switching transistor have a higher threshold voltage than the switching transistors, the channel width of the storage

transistors and the first power switch transistor is less than the thickness of the gate insulating layer of the switching transistors.

Regarding claims 34-37, figure 6 of Oklobdzija et al. reference shows of the pulse generator comprises inverters having transistors with low threshold voltages.

Regarding claims 30-32 and 52-53, figures 16 and 17 of Matsuzaki et al. reference teaches that leakage current in a logic circuit can be reduced by implementing a power switch in either configuration. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to include an additional power transistor for coupling/decoupling the switching transistors of Oklobdzija et al. reference to/from the power supply for the purpose of reducing power consumption.

7. Claims 39-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oklobdzija et al. (USP 6,232,810) in view of Matsuzaki et al. (USP 6,500,715) in further view of Sani et al. (USP 6,794,914).

The combination of Oklobdzija et al. and Matsuzaki et al. references discloses an circuit arrangement comprising all the aspects of the present invention as noted in the above except for the test circuit coupled to the flip flop for testing the functionality of the flip flop as called for in claim 39.

Sani et al. shows a flip flop having a test circuit (310 of figure 3) to test and to enhance the reliability of the flip flop. Therefore, it would have been obvious to a person skilled in the art at the time the invention was made to include Sani et al.'s test circuit in the circuit arrangement of Oklobdzija et al. And Matsuzaki et al. references for purpose of enhancing the reliability of the flip flop.

Regarding claim 40, the combination of Oklobdzija et al., Matsuzaki et al. and Sani et al. references show the test circuit comprising a test input signal (Sin), output components (output of the flip flop) that reads a test output signal of the flip flop.

Regarding claim 41, the combination of Oklobdzija et al., Matsuzaki et al. and Sani et al. references show the test circuit comprising a plurality of transistors (322, 324) having a high threshold voltage.

Regarding claim 42, since test transistors have a higher threshold voltage than the threshold voltage of the switching transistors, the thickness of the gate insulating layer of the test transistors are greater than the thickness of the gate insulating layer of the switching transistors.

Regarding claims 43-44, since test transistors have a higher threshold voltage than the threshold voltage of the pulse generator's transistors, the thickness of the gate insulating layer of the test transistors are greater than the thickness of the gate insulating layer of the pulse generator's transistors.

Response to Arguments

8. Applicant's arguments filed 12/22/2008 have been fully considered but they are not persuasive.

Claims 25, 27-29, 34-37 and 45-50 as being anticipated by Inukai et al, hereinafter "Inukai":

Applicant argues that Inukai reference does not couple a flip flop input signal into the storage flip flop subcircuit as called for in claim 29 is not persuasive. Webster's II University Dictionary defines couple/coupling as something that units or connects two thing together: LINK. Thus, the switching transistors within the NANDS certainly

connect the flip flop input signal (input applied to the NAND gates) to the storage flip flop subcircuit. Therefore, the limitations a plurality of switching transistors for coupling a flip flop input signal into the storage flip flop subcircuit is fully met.

Applicant argues that the set reset crossed coupled NAND gates do not have a defined electrical potential in an operating state in which at least one supply voltage of the circuit arrangement is switched off as claim 29 requires is not persuasive. In the operating state, the Stand-by signal switches off the power switch, the crossed coupled NAND gates coupled to a defined electrical potential GNDV. The set and reset terminals receive the flip flop input signal with predefined potential. Therefore, the limitation of each of the terminals of the switching transistors has a defined electrical potential in the operating state is fully met.

Applicant argues that the six transistors on the right hand side receiving High Vdd in figure 9 of Inukai is not a storage flip flop of an edge triggered flip flop is not persuasive. Figure 9 of Inukai shows an edge triggered flip flop (flip flop triggered by a clock signal CLK) comprising a storage flip flop circuit (the six transistors on the right hand side receiving High Vdd). Therefore, the limitations of an edge triggered flip flop comprising a storage flip flop circuit is fully met.

Since Inukai reference shows all limitations as claim 29 requires, dependent claims 25, 27-28, 34-37 and 45-50 are also rejected for the reasons as noted above.

Claims 52-53 are rejected under 35USC 103(a) as being unpatentable over Inukai in view of Matsuzaki:

Since Inukai reference shows all limitations as claim 29 requires, claims 52-53 require similar limitations, are also rejected as being unpatentable over Inukai in view of Matsuzaki for the reasons as noted above.

Claims 30-32 are rejected under 35USC 103(a) as being unpatentable over Inukai in view of Matsuzaki; claims 39-44 are rejected under 35USC 103(a) as being unpatentable over Inukai in view of Sani:

Since Inukai reference shows all limitations as claim 29 requires, dependent claims 30-32 and 39-44 are also rejected for the reasons as noted above.

Claims 25, 27-32, 34-37 and 52-53 are rejected under 35USC 103(a) as being unpatentable over Oklobdzija et al. in view of Matsuzaki et al.:

Applicant argues that the first and second logic blocks (34 and 36 of Oklobdzija's figure 6A) does not couple a flip flop input into a storage flip flop subcircuit as claim 29 requires is not persuasive. Webster's II University Dictionary defines couple/coupling as something that units or connects two thing together: LINK. Thus, the switching transistors within the first and second logic blocks (34 and 36) certainly connect the flip flop input signal (signals on signal lines 38 and 40) to the storage flip flop subcircuit. Therefore, the limitations a plurality of switching transistors for coupling a flip flop input signal into the storage flip flop subcircuit is fully met.

Applicant argues that the switching transistors does not have a defined electrical potential when at least one supply voltage is switched off is not persuasive. In the operating state, the Stand-by signal switches off the power switch (see above for the details of the rejection), the each of terminals of the switching transistors has a defined electrical potential (gate terminals receive the flip flop input signals from signal lines 38, 40, source/drain coupled to Vdd, drain source coupled to signal Q, Q/). Therefore, the limitations of the switching transistors have a defined electrical potential when at least one supply voltage is switched off is fully met.

Since the combination of Inukai and Matsuzaki et al. references shows all limitations as claim 29 requires, dependent claims 25, 27-28 and 34-37 are also rejected for the reasons as noted above.

Since Inukai and Matsuzaki et al. references shows all limitations as claim 29 requires, claims 52-53 require similar limitations, are also rejected as being unpatentable over Inukai in view of Matsuzaki for the reasons as noted above

Claims 39-44 are rejected under 35USC 103(a) as being unpatentable over Oklobdzija et al. in view of Matsuzaki et al. in further view of Sani et al.:

Since Inukai reference shows all limitations as claim 29 requires, dependent claims 39-44 require similar limitations, are also rejected as being unpatentable over Inukai in view of Matsuzaki and further view of Sani et al. for the reasons as noted above

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tuan T. Lam/
Primary Examiner, Art Unit 2816

2/5/2009